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EXAMINER	
GOLDEN, JAMES R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,223	ITO ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/699223 has a total of 12 claims pending. There are 2 independent claims and 9 dependent claims.

Drawings

1. The corrections to the drawings received in the amendment dated 05/03/2006 are accepted, and the objections are withdrawn.

Specification

2. The correction to the title received in the amendment dated 05/03/2006 is accepted, and the objection is withdrawn.

3. The corrections to the abstract received in the amendment dated 05/03/2006 are accepted, and the objections are withdrawn.

4. The corrections to the specification received in the amendment dated 05/03/2006 are accepted, and the objections are withdrawn.

Claim Objections

5. The corrections to the claims received in the amendment dated 05/03/2006 are accepted, and the objections are withdrawn.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1 and 3-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al. (US 2003/0061536).

8. **With respect to claim 1**, Nakai et al. disclose a semiconductor integrated circuit device having a dynamic RAM, said dynamic RAM comprising a memory array (11_1, 11_2, 11_3 and 11_4 of Fig. 1) [0005; 0083, "In Fig. 1, same reference numbers are assigned to corresponding parts having some functions as in Fig. 13"], a RAM control section (21 of Fig. 1) [0084], an ECC-codec circuit (24 of Fig. 1) [0085, lines 9-10, 17], and an ECC controller (23 of Fig. 1) [0083], said RAM control section comprising a command decoding section responsive to an external command from the outside of said dynamic RAM for decoding the external command [0037; 0084, lines 13-21; super self-refresh is synonymous with "ultra low-power consumption mode"] and a super self-refresh control circuit (22 of Fig. 1) [0083, line 9], said super self-refresh control circuit being contained within said RAM control section (making a component integral is "merely a matter of obvious engineering choice" and therefore unpatentable, according to *MPEP 2144.04 V B*; see response to arguments below at paragraph 25), wherein:

- said command decoding section is also adapted to receive an internal command generated inside said dynamic RAM and to decode the internal command [0091, lines 1-3, 12-15];
- said ECC controller (23 of Fig. 1) [0083] comprises a command generating section (23 of Fig. 1) and an address generating section (9 of Fig. 1) [0091, lines 1-3; controller generates "an internal command" and "an address"], said address generating section being contained within said ECC controller (making a component integral is "merely a matter of obvious engineering choice" and therefore unpatentable, according to *MPEP 2144.04 V B*; see response to arguments below at paragraph 25);
- said command decoding section delivers a start instruction signal representative of encoding to said ECC controller when an entry command is decoded as the external command [0084, lines 4-21];
- said command generating section of said ECC controller delivers, upon reception of the start instruction signal, a first operation mode signal representative of the encoding and simultaneously makes said address generating section of said ECC controller sequentially generate addresses corresponding to operation timings of the first operation mode signal [0084, lines 3-21; 0101, lines 1-13; encode start signal ENST is generated to put the device in self-refreshing ultra low-power consumption mode] and supplies the addresses to said memory array [0010, lines 7-15; 0104, lines 1-6; refresh counter generates addresses].

- said ECC-codec circuit carries out, upon reception of the first operation mode signal, an encoding operation of producing a check bit for error detection/correction with reference to information data stored in said memory array and writes the check bit into a predetermined region of said memory array [0092, lines 1-7];
- said command generating section of said ECC controller delivers, upon completion of the encoding operation by said ECC-codec circuit, a first end signal as the internal command to said command decoding section [0091, lines 15-20];
- said super self-refresh control circuit of said RAM control section starts, when said command decoding section receives and decodes the first end signal as the internal command, a super self-refresh operation which has a refresh cycle lengthened within an allowable range of error occurrence by an error correcting operation using the check bit [0080; 0088, lines 1-6; 0101, line 19 -- 0102].

9. **With respect to claim 3**, Nakai et al. disclose a semiconductor integrated circuit device as claimed in claim 1 (see above paragraph 0), wherein:

- said command decoding section delivers, when an exit command as the external command is decoded, a stop instruction signal representative of decoding to said ECC controller [0091, lines 20-31];
- said super self-refresh control circuit of said RAM control section finishes the super self-refresh operation when said command decoding section decodes the exit command [0108, line 1 -- 0109, line 7];

- said command generating section of said ECC controller delivers, upon reception of the stop instruction signal, a second operation mode signal representative of the decoding and simultaneously makes said address generating section of said ECC controller sequentially generate addresses corresponding to operation timings of the second operation mode signal [0084, lines 3-21; 0101, lines 1-13; encode start signal ENST is generated to put the device in self-refreshing ultra low-power consumption mode] and supplies the addresses to said memory array [0010, lines 7-15; 0104, lines 1-6; refresh counter generates addresses];
- said ECC-codec circuit carries out, upon reception of the second operation mode signal, a decoding operation of reading the check bit for error detection/correction from the predetermined region of said memory array and corrects, with reference to the check bit and the information data stored in said memory array, an error in the information data to rewrite the information data [0092, lines 7-12; 0109, lines 10-22];
- said command generating section of said ECC controller delivers, upon completion of the decoding operation by said ECC-codec circuit, a second end signal as the internal command to said command decoding section [0109, lines 22-32].

10. **With respect to claim 4**, Nakai et al. disclose a semiconductor integrated circuit device as claimed in claim 3 (see above paragraph 9), wherein: said RAM control section automatically starts a self-refresh operation and holds data in response to the second end signal [0109, lines 22-32; 0110].

11. **Claims 2 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al. (US 2003/0061536) as applied to claims 1 and 3-4 above (see above paragraphs 0 and 9-10), and further in view of Attaway et al. (US 6,829,677).

12. **With respect to claim 2**, Nakai et al. disclose the semiconductor integrated circuit device as claimed in claim 1 (see above paragraph 0). Nakai et al. do not disclose the limitation wherein the entry command is supplied by a user to said dynamic RAM.

However, Attaway et al. disclose the limitation wherein the entry command is supplied by a user to said dynamic RAM (column 3, lines 35-45).

Nakai et al. and Attaway et al. are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes. At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the DRAM of Nakai et al. with the self-refresh state entry command that may be entered by the user of Attaway et al. The motivation for doing so would have been because "there may be contents in the SDRAM memory which the user may wish to preserve for use after the system has been reset" (column 8, lines 15-17).

Therefore, it would have been obvious to combine Attaway et al. with Nakai et al. for the benefit of a DRAM with a self-refresh state entry command that may be entered by the user to obtain the invention as specified in claim 2.

13. **With respect to claim 5**, Nakai et al. disclose a semiconductor integrated circuit device as claimed in claim 3 (see above paragraph 9). Nakai et al. do not disclose the

limitation wherein said RAM control section subsequently receives a refresh operation instruction from the outside and holds data.

However, Attaway et al. disclose the limitation wherein said RAM control section subsequently receives a refresh operation instruction from the outside and holds data (column 3, lines 35-45).

Nakai et al. and Attaway et al. are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes. At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the DRAM of Nakai et al. with the self-refresh state entry command that may be entered by the user of Attaway et al. The motivation for doing so would have been because "there may be contents in the SDRAM memory which the user may wish to preserve for use after the system has been reset" (column 8, lines 15-17).

Therefore, it would have been obvious to combine Attaway et al. with Nakai et al. for the benefit of a DRAM with a self-refresh state entry command that may be entered by the user to obtain the invention as specified in claim 5.

14. **Claim 6** is rejected under 35 U.S.C. 103(a) as being anticipated over Nakai et al. (US 2003/0061536) as applied to claims 1 and 3-4 above (see paragraphs 0 and 9-10), and further in view of Sawhney (US 2002/0133663).

15. **With respect to claim 6**, Nakai et al. disclose the semiconductor integrated circuit device as claimed in claim 3 (see above paragraph 9). Nakai et al. do not disclose the limitation wherein the entry command and the exit command are supplied by a user to said dynamic RAM.

However, Attaway et al. disclose the limitation wherein the entry command is supplied by a user to said dynamic RAM (column 3, lines 35-45).

Nakai et al. and Attaway et al. are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes. At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the DRAM of Nakai et al. with the self-refresh state entry command that may be entered by the user of Attaway et al. The motivation for doing so would have been because "there may be contents in the SDRAM memory which the user may wish to preserve for use after the system has been reset" (column 8, lines 15-17).

Therefore, it would have been obvious to combine Attaway et al. with Nakai et al. for the benefit of a DRAM with a self-refresh state entry command that may be entered by the user to obtain the invention as specified in claim 6.

Additionally, Ito et al disclose the limitation wherein the exit command is supplied by a user to said dynamic RAM [0033, lines 1-11].

Sawhney and Attaway et al. are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes. At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the DRAM of Nakai et al. with the self-refresh state exit command that may be entered by the user of Sawhney. The motivation for doing so would have been because "after a refresh end event occurs, the refresh operation on memory section 201 ends and ISOa is re-energized" [0042, lines 26-28], and only once ISOa is re-energized can memory access occur.

Therefore, it would have been obvious to combine Sawhney with Nakai et al. for the benefit of a DRAM with a self-refresh state entry command that may be entered by the user to obtain the invention as specified in claim 6.

16. **Claims 7 and 9-11** are rejected under 35 U.S.C. 103(a) as being anticipated over Nakai et al. (US 2003/0061536) as applied to claims 1 and 3-4 above (see above paragraphs 0 and 9-10), and further in view of Dell (US 5,450,422).

17. **With respect to claim 7**, Nakai et al. disclose a semiconductor integrated circuit device having a dynamic RAM, said dynamic RAM comprising a memory array (11_1, 11_2, 11_3 and 11_4 of Fig. 1) [0005; 0083, "In Fig. 1, same reference numbers are assigned to corresponding parts having some functions as in Fig. 13"], a RAM control section (21 of Fig. 1) [0084], an error correction circuit (24 of Fig. 1) [0085, lines 9-10, 17], and a BIST (built-in self-test) controller (23 of Fig. 1) [0083], said RAM control section comprising a command decoding section responsive to an external command from the outside of said dynamic RAM for decoding the external command [0037; 0084, lines 13-21; super self-refresh is synonymous with "ultra low-power consumption mode"], wherein:

- said command decoding section is also adapted to receive an internal command generated inside said dynamic RAM and to decode the internal command [0091, lines 1-3, 12-15];
- said BIST controller (23 of Fig. 1) [0083] comprises a command generating section (23 of Fig. 1) and an address generating section (9 of Fig. 1) [0091, lines 1-3; controller generates "an internal command" and "an address"], said address

generating section being contained within said BIST controller (making a component integral is "merely a matter of obvious engineering choice" and therefore unpatentable, according to *MPEP 2144.04 V B*; see response to arguments below at paragraph 25);

- said command decoding section delivers a start instruction signal representative of checking to said BIST controller when an entry command is decoded as the external command [0085, lines 1-20; BIST controller enters decode state] [0092, lines 7-12; BIST controller checks for parity errors and corrects them];
- said command generating section of said BIST delivers, upon reception of the start instruction signal, an operation mode signal representative of the checking command [0085, lines 1-20; BIST controller enters decode state] [0092, lines 7-12; BIST controller checks for parity errors and corrects them] and simultaneously makes said address generating section of said BIST controller sequentially generate addresses corresponding to operation timings of the first operation mode signal and supplies the addresses to said memory array [0010, lines 7-15; 0104, lines 1-6; refresh counter generates addresses].
- said error correction circuit produces, upon reception of the operation mode signal, write data corresponding to the addresses sequentially generated, writes the write data into a predetermined region or an entire region of said memory array [0092, lines 1-7],
- upon completion of error detection, delivers an end signal as the internal command to said command decoding section [0109, lines 22-27];

- delivery of the start instruction signal being stopped when said command decoding section receives and decodes the end signal as the internal command [0109, lines 27-28].

Nakai et al. do not disclose the limitation wherein said error correction circuit

- produces expectation data corresponding to the addresses sequentially generated, compares the expectation data with the information data read from said memory array, detects an error in the information data.

However, Dell discloses the limitation wherein said error correction circuit

- produces expectation data corresponding to the addresses sequentially generated (column 7, lines 5-7), compares the expectation data with the information data read from said memory array (column 7, lines 8-10), detects an error in the information data (column 7, lines 13-15).

Nakai et al. and Dell are analogous art because they are from the same field of endeavor, namely DRAM error detection and correction.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the specific error detection and correction scheme of Dell to the DRAM of Nakai et al. The motivation for doing so would have been because the scheme of Dell allows for the "generation of syndrome bits" and a table of "the errors which [the syndrome bits] indicate" (column 7, lines 13-15).

Therefore, it would have been obvious to combine Dell with Nakai et al. for the benefit of a DRAM with an error detection and correction scheme to obtain the invention as specified in claim 7.

18. **With respect to claim 9**, Nakai et al. in view of Dell disclose a semiconductor integrated circuit device as claimed in claim 7 (see above paragraph 17). Nakai et al. in view of Dell do not disclose

- said BIST controller further comprises a register circuit which holds the result of the error detection;
- said BIST controller makes said register circuit deliver the result of error detection to the outside when said command decoder receives a readout instruction as the external command.

However, Dell discloses the limitations wherein

- said BIST controller (13 of Fig. 1; column 3, lines 33-37) further comprises a register circuit which holds the result of the error detection (52 of Fig. 7; column 7, lines 10-13; the syndrome bits are the result of the error detection, and they are generated and output by the comparator, so therefore the comparator output is functionally equivalent to a register);
- said BIST controller (13 of Fig. 1) making said register circuit (52 of Fig. 1) deliver the result of error detection (column 7, lines 49-51; the syndrome bits are passed on to the corrector outside of the memory) to the outside when said command decoder (20 of Fig. 1; column 3, lines 54-57) receives a readout instruction as the external command (column 3, lines 33-37, lines 57-62; the CPU that is external to the memory requests a read from memory).

Nakai et al. and Dell are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the read mechanism of error detection data of Dell to the DRAM of Nakai et al. The motivation for doing so would have been because the correction data can be utilized such that "all single-bit errors can be detected and hence corrected" (column 7, lines 40-41).

Therefore, it would have been obvious to combine the Dell with Nakai et al. for the benefit of a read mechanism of error detection data in a DRAM to obtain the invention as specified in claim 9.

19. **With respect to claim 10**, Nakai et al. disclose a semiconductor integrated circuit device as claimed in claim 3 (see above paragraph 9). Nakai et al. in view of Dell do not disclose

- said ECC-codec circuit further comprises a register circuit which holds an error detection signal of said ECC-codec circuit as a result of error detection;
- said ECC-codec circuit makes said register circuit deliver the result of error detection to the outside when said command decoder receives a readout instruction as the external command.

However, Dell discloses the limitations wherein

- said ECC-codec circuit (13 of Fig. 1; column 3, lines 33-37) further comprises a register circuit which holds an error detection signal of said ECC-codec circuit as a result of error detection (52 of Fig. 7; column 7, lines 10-13; the syndrome bits are the result of the error detection, and they are generated and output by the

comparator, so therefore the comparator output is functionally equivalent to a register);

- said ECC-codec circuit (13 of Fig. 1) making said register circuit (52 of Fig. 1) deliver the result of error detection (column 7, lines 49-51; the syndrome bits are passed on to the corrector outside of the memory) to the outside when said command decoder (20 of Fig. 1; column 3, lines 54-57) receives a readout instruction as the external command (column 3, lines 33-37, lines 57-62; the CPU that is external to the memory requests read from memory).

Nakai et al. and Dell are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the read mechanism of error detection data of Dell to the DRAM of Nakai et al. The motivation for doing so would have been because the correction data can be utilized such that "all single-bit errors can be detected and hence corrected" (column 7, lines 40-41).

Therefore, it would have been obvious to combine the Dell with Nakai et al. for the benefit of a read mechanism of error detection data in a DRAM to obtain the invention as specified in claim 10.

20. **With respect to claim 11**, Nakai et al. in view of Dell disclose a semiconductor integrated circuit device as claimed in claim 3 (see above paragraph 9). Nakai et al. in view of Dell do not disclose

- said ECC controller further comprises a register circuit which holds an error location detection instruction of said ECC controller as a result of the error detection;
- said ECC controller makes said register circuit deliver the result of error detection to the outside when said command decoder receives a readout instruction as the external command.

However, Dell discloses the limitations wherein

- said ECC controller (13 of Fig. 1; column 3, lines 33-37) further comprises a register circuit which holds an error location detection instruction of said ECC controller as a result of the error detection (52 of Fig. 7; column 7, lines 10-13; the syndrome bits are the result of the error detection, and they are generated and output by the comparator, so therefore the comparator output is functionally equivalent to a register);
- said ECC controller (13 of Fig. 1) making said register circuit (52 of Fig. 1) deliver the result of error detection (column 7, lines 49-51; the syndrome bits are passed on to the corrector outside of the memory) to the outside when said command decoder (20 of Fig. 1; column 3, lines 54-57) receives a readout instruction as the external command (column 3, lines 33-37, lines 57-62; the CPU that is external to the memory requests read from memory).

Nakai et al. and Dell are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the read mechanism of error detection data of Dell to the DRAM of Nakai et al. The motivation for doing so would have been because the correction data can be utilized such that "all single-bit errors can be detected and hence corrected" (column 7, lines 40-41).

Therefore, it would have been obvious to combine the Dell with Nakai et al. for the benefit of a read mechanism of error detection data in a DRAM to obtain the invention as specified in claim 11.

21. **Claim 8** is rejected under 35 U.S.C. 103(a) as being anticipated over Nakai et al. (US 2003/0061536) in view of Dell (US 5,450,422) as applied to claims 7 and 9-11 above (see paragraphs 17 and 18-20), and further in view of Attaway et al. (US 6,829,677).

22. **With respect to claim 8**, Nakai et al. in view of Dell disclose a semiconductor integrated circuit device as claimed in claim 7 (see paragraph 17). Nakai et al. in view of Dell do not disclose the limitation wherein the BIST entry command is supplied by a user to said dynamic RAM.

However, Attaway et al. disclose the limitation wherein the entry command is supplied by a user to said dynamic RAM (column 3, lines 35-45).

Nakai et al. and Attaway et al. are analogous art because they are from the same field of endeavor, namely DRAM refresh schemes. At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the DRAM of Nakai et al. with the self-refresh state entry command that may be entered by the user of

Attaway et al. The motivation for doing so would have been because "there may be contents in the SDRAM memory which the user may wish to preserve for use after the system has been reset" (column 8, lines 15-17).

Therefore, it would have been obvious to combine Attaway et al. with Nakai et al. for the benefit of a DRAM with a self-refresh state entry command that may be entered by the user to obtain the invention as specified in claim 8.

23. **Claim 12** is rejected under 35 U.S.C. 103(a) as being anticipated over Nakai et al. (US 2003/0061536) as applied to claims 1 and 3-4 above (see paragraphs 0 and 9-10), and further in view of Saiki et al. (JP 362078920).

24. **With respect to claim 12**, Nakai et al. in view of Dell disclose a semiconductor integrated circuit device as claimed in claim 3 (see above paragraph 9) wherein a sequential decoding is used in decoding an error correction code in said super self-refresh operation [100]. Nakai et al. in view of Dell do not disclose the limitation error location detection being executed by backward cyclic shift of a cyclic shift register, other operations being executed by forward cyclic shift.

However, Saiki et al disclose the limitation error location detection being executed by backward cyclic shift of a cyclic shift register, other operations being executed by forward cyclic shift ("Constitution" section of English-language translation). At the time of invention it would have been obvious to combine the error-correcting shift register of Saiki et al. with the DRAM of Nakai et al. in view of Dell. The motivation for doing so would have been because the bits "represent an error pattern" which can be

used "to correct the error of the received code" ("Constitution" section of English-language translation).

Therefore, it would have been obvious to combine Saiki et al. with Nakai et al. in view of Dell for the benefit of a DRAM with an error-correcting shift register to obtain the invention specified in claim 12.

Response to Arguments

25. Applicant's arguments filed 05/03/2006 have been fully considered but they are not persuasive.

26. **With respect to applicant's arguments regarding claim 1**, the new limitations "said super self-refresh control circuit being contained within said RAM control section" and "said address generating section being contained within said ECC controller" fail to distinguish the claimed subject matter over prior art. Making a component integral to another component is an unpatentable variation. The Examiner refers applicant to *MPEP 2144.04 V B*:

"*In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) (A claim to a fluid transporting vehicle was rejected as obvious over a prior art reference which differed from the prior art in claiming a brake drum integral with a clamping means, whereas the brake disc and clamp of the prior art comprise several parts rigidly secured together as a single unit. The court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."); but see *Schenck v.*

Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983) (Claims were directed to a vibratory testing machine (a hard-bearing wheel balancer) comprising a holding structure, a base structure, and a supporting means which form "a single integral and gaplessly continuous piece." Nortron argued that the invention is just making integral what had been made in four bolted pieces. The court found this argument unpersuasive and held that the claims were patentable because the prior art perceived a need for mechanisms to dampen resonance, whereas the inventor eliminated the need for dampening via the one-piece gapless support structure, showing insight that was contrary to the understandings and expectations of the art.)."

Therefore, the rejection to claim 1 stands as issued.

27. **With respect to applicant's arguments regarding claims 3-4**, see the above response to the argument regarding claim 1 (paragraph 26). The rejections to claims 3-4 stand as issued.

28. **With respect to applicant's arguments regarding claims 2 and 5**, see the above response to the argument regarding claim 1 (paragraph 26). The rejections to claims 2 and 5 stand as issued.

29. **With respect to applicant's arguments regarding claim 6**, see the above response to the argument regarding claim 1 (paragraph 26). The rejection to claim 6 stands as issued.

30. **With respect to applicant's arguments regarding claim 7**, the new limitation "said address generating section being contained within said BIST controller" fails to distinguish the claimed subject matter over prior art. Making a component integral to

another component is an unpatentable variation. See the above response to the argument regarding claim 1 (paragraph 26). The rejection to claim 7 stands as issued.

31. **With respect to applicant's arguments regarding claim 9**, see the above response to the argument regarding claim 7 (paragraph 30). The rejection to claim 9 stands as issued.

32. **With respect to applicant's arguments regarding claims 10-11**, see the above response to the argument regarding claim 1 (paragraph 26). The rejections to claims 10-11 stand as issued.

33. **With respect to applicant's arguments regarding claim 8**, see the above response to the argument regarding claim 7 (paragraph 30). The rejection to claim 9 stands as issued.

34. **With respect to applicant's arguments regarding claim 12**, see the above response to the argument regarding claim 1 (paragraph 26). The rejection to claim 9 stands as issued.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

July 23, 2006

Brian R. Pough
Primary Examiner